Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A phase change memory device, comprising:

a substrate;

a first electrode disposed over the substrate;

phase change material disposed over and in electrical contact with the first electrode;

a second electrode disposed over and in electrical contact with the phase change material, wherein electrical current passing through the first and second electrodes and the phase change material generates heat for heating the phase change material; and

insulation material disposed adjacent to the phase change material, wherein a void is formed in the insulation material to impede heat from the phase change material from conducting through the insulation material.

2. (Original) The phase change memory device of claim 1, wherein the insulation material includes:

at least one layer of insulation material having a hole formed therein, wherein at least a portion of the phase change material is disposed in the hole; and

spacer material disposed in the hole.

3. (Original) The phase change memory device of claim 2, wherein the void is formed in the spacer material.

4. (Original) The phase change memory device of claim 1, wherein the void is an annularly shaped trench that laterally surrounds at least a portion of the phase change material.

5. (Original) The phase change memory device of claim 4, wherein the void is directly adjacent to the phase change material.

6. (Original) The phase change memory device of claim 4, wherein the void is indirectly adjacent to the phase change material.

7. (Original) The phase change memory device of claim 1, wherein the substrate is semiconductor material having a first conductivity type, and the memory device further comprises:

first and second spaced-apart regions formed in the substrate and having a second conductivity type, with a channel region defined in the substrate therebetween; and

a third block of conductive material disposed over and insulated from the channel region;

wherein the first block is disposed over and electrically connected to the first region.

8. (Original) The phase change memory device of claim 2, wherein:

the spacer material has a surface that defines an opening having a width that narrows along a depth of the opening;

the first electrode is a first block of conductive material disposed in the hole;

the phase change material is a layer disposed in the opening and extending along the spacer material surface and along at least a portion of an upper surface of the first block;

the second electrode is a second block of conductive material disposed in the opening and on the phase change material layer; and

the second block of material and the phase change material layer form an electrical current path that narrows in width as the current path approaches the first block upper surface.

9. (Original) The phase change memory device of claim 8, wherein the spacer material surface is generally funnel-shaped.

10. (Original) The phase change memory device of claim 8, wherein the current path reaches a minimum cross sectional area adjacent the first block upper surface.

11. (Original) The phase change memory device of claim 8, wherein the first block of conductive material is disposed in the opening defined by the spacer material surface.

12. (Original) The phase change memory device of claim 8, wherein the spacer material is formed over the first block upper surface.

13. (Original) The phase change memory device of claim 12, wherein an indentation is formed into the first block upper surface, and a portion of the phase change material layer extends into the indentation.

14. (Original) The phase change memory device of claim 13, wherein a portion of the second block extends into the indentation.

15. (Original) The phase change memory device of claim 8, wherein the phase change material layer merges together to form a column of the phase change material disposed directly over the first block upper surface.

16. (Original) The phase change memory device of claim 15, wherein the current path reaches a minimum cross sectional area at the column.

Claims 17-52: (Currently Cancelled).

53. (Original) An array of phase change memory devices, comprising:
a substrate;
a plurality of first electrodes disposed over the substrate;

phase change material disposed over and in electrical contact with the first electrodes;

a plurality of second electrodes disposed over and in electrical contact with the phase change material, wherein electrical current passing through the first and second electrodes and the phase change material generates heat for heating the phase change material; and

insulation material disposed adjacent to the phase change material, wherein a plurality of voids are formed in the insulation material to impede heat from the phase change material from conducting through the insulation material.

54. (Original) The array of claim 53, wherein the insulation material includes:

at least one layer of insulation material having a plurality of holes formed therein, wherein at least portions of the phase change material are disposed in the holes; and

spacer material disposed in the holes.

55. (Original) The array of claim 54, wherein the voids are formed in the spacer material.

56. (Original) The array of claim 53, wherein the voids are annularly shaped trenches that laterally surround portions of the phase change material.

57. (Original) The array of claim 56, wherein the voids are directly adjacent to the phase change material.

58. (Original) The array of claim 56, wherein the voids are indirectly adjacent to the phase change material.

59. (Original) The array of claim 53, wherein the substrate is semiconductor material having a first conductivity type, and the array further comprising:

a plurality of first and second spaced-apart regions formed in the substrate and having a second conductivity type, with channel regions of the substrate defined between the first and second regions; and

a plurality of third blocks of conductive material each disposed over and insulated from one of the channel regions;

wherein the first blocks are each disposed over and electrically connected to one of the first regions.

60. (Original) The array of claim 54, wherein:

the spacer material includes surfaces that define openings having widths that narrow along depths of the openings;

the first electrodes are first blocks of conductive material each disposed in one of the holes;

the phase change material extends along the spacer material surfaces and along at least portions of upper surfaces of the first blocks;

the second electrodes are second blocks of conductive material disposed in the openings and on the phase change material; and

the second blocks of material and the phase change material form electrical current paths that narrow in width as the current paths approach the first block upper surfaces.

61. (Original) The array of claim 60, wherein the spacer material surfaces are generally funnel-shaped.

62. (Original) The array of claim 60, wherein the current paths reach minimum cross sectional areas adjacent the first block upper surfaces.

63. (Original) The array of claim 60, wherein the first blocks of conductive material are disposed in the opening defined by the spacer material surfaces.

64. (Original) The array of claim 60, wherein the spacer material is formed over the first block upper surfaces.

65. (Currently Amended) The array of claim ~~[65]~~ 64, wherein indentations are formed into the first block upper surfaces, and portions of the phase change material extend into the indentations.

66. (Currently Amended) The array of claim ~~[66]~~ 65, wherein portions of the second blocks extend into the indentations.

67. (Original) The array of claim 60, wherein the phase change material is at least one layer of material that merges together to form columns of the phase change material disposed directly over the first block upper surfaces.

68. (Original) The array of claim 67, wherein the current paths reach minimum cross sectional areas at the columns.

Claims 69-86: (Currently Cancelled).